Amendments to the Specification:

[0013] An ~~Object~~ object of the present invention is to completely planarize the surface of a member which has been polished by the CMP method.

[0022]In addition, the semiconductor integrated circuit device according to the present invention comprises ~~ashallow~~ a shallow trench formed on the principal surface of a semiconductor substrate, an element isolation region having an insulating film, which contains a film planarized by the CMP method, embedded in the shallow trench, and active regions of the semiconductor integrated circuit element separated by said element isolation region, wherein dummy regions, which do not function as a semiconductor integrated circuit element, are formed on the principle surface of the semiconductor substrate in an empty space of the semiconductor substrate between said spaced active regions.

[0026]Incidentally, examples of the interconnection include ~~-~~a metal interconnection formed on an interlayer insulating film, a gate interconnection of a MISFET (Metal-Insulator- Semiconductor Field Effect Transistor) and a bit line of a DRAM (Dynamic Random Access Memory). It is needless to say that not only the interconnection of memory devices, such as a DRAM, but also the interconnection of logic devices, are included in the metal interconnection and gate interconnection. In particular, the logic device generally has a multilayer interconnection formed of at least three layers so that the application of the present invention to such an interconnection brings about marked effects.

[0039] (3) In a further aspect, the semiconductor integrated ~~F.~~ circuit device

according to the present invention is similar to the above-described one except that, in the same interconnection layer which includes a bonding pad portion or marker portion for photolithography disposed on the semiconductor substrate, dummy interconnections are not formed at the periphery of the bonding pad portion or a marker portion.

[0044] Described more specifically, in the fabrication process according to the present invention, the concave portions formed between the actual interconnections and dummy interconnections are filled in with the first insulating film composed of a silicon oxide film formed by the SOC or high-density plasma CVD method, a BPSG or PSG film formed by the re-flow method or a polysilazane film, whereby the unevenness remaining on the surface of the second insulating film is lessened compared with the unevenness before the formation of the film. Accordingly, the thickness of the second ~~insulting~~ insulating film must be sufficient for the planarization of the unevenness on the surface of the first insulating film, but the surface of the second insulating film can be planarized sufficiently even by a thin film.

[0045] (4) Incidentally, a rigid pad can be used for said CMP polishing. Alternatively, polishing by the CMP method can be employed only for the surface finish polishing after the unevenness on the surface attributable to the existence of the actual interconnections and dummy interconnections is substantially planarized by the first and second ~~insulatingfilms~~ insulating films. As a polishing means employed for the surface finish, not only the CMP method, but also other polishing means, such as dry belt polishing and lapping, may be used.

[0094]A portion of the gate interconnection 6 is formed to extend over the element separation region 3 and another portion is formed to be a gate electrode 7 of a MISFETQ1 formed in the active region 4 of the semiconductor substrate 1. On both sides of the gate electrode 7 in the active regions 4 on the principal surface of the semiconductor substrate 1, impurity semiconductor regions ~~S~~ 8 are formed. The impurity semiconductor regions 8 function as a source drain region for the MISFETQ1. It is also possible to employ the region 8 as a so-called LDD (Lightly Doped Drain). On the side of the gate interconnection 6, a side wall spacer 8b is formed. The side wall spacer 8b can be formed of a silicon oxide film or a silicon nitride film.

[0101]The member space ~~5~~ S, which is a space between the interconnection 10 and the dummy interconnection 11, or a space between adjacent dummy interconnections 11, is not greater than twice the height of the interconnection height H of the dummy interconnection 11 or interconnection 10. As described above with reference to Fig. 30, by setting the member space S at not greater than twice the interconnection height H, the CMP polishing amount of the insulating film 12 can be made uniform and the surface of the insulating ~~film12~~ film 12 can be completely planarized. In a region not wider than 5% of the chip area, the member space S is allowed to have a height of at most four times the interconnection height H. In this case, although the fluctuations of the polishing amount of the insulating film 12 increase about twice, they can be neglected as a whole because this area amounts to not greater than 5% of the chip area. The flatness of the whole insulating film 12 therefore can be substantially maintained.

[0102] In addition, as the member space ~~5~~ S, a space not smaller than the

minimum space width required by a lithographic tool is necessary. This condition permits accurate processing of the interconnection 10 and dummy interconnection 11, whereby each member can be processed accurately according to the design. In the case of an exposure apparatus using a KRF exima laser as a light source, 0.2 μm can be given as an example of the minimum space width.

[0103]The width (a) of the dummy interconnection 11 is set to be not smaller than the minimum line width required by a lithographic tool. By setting the width (a) to be not smaller than the minimum line width, the dummy interconnections 11 can be processed with certainty. In the scribing area, the width (a) of each of the dummy interconnections 11 is set at not greater than the distance between bonding pads 13. By doing so, even if the dummy interconnections 11 are peeled off into minute chips by dicing or the like and produce conductive dust, no short circuit occurs between the bonding pads 13, which makes it possible to eliminate a cause for possible failure. The width (a) of each of the dummy interconnections 11 is ~~set~~ set to be, for example, not greater than 30 μm, with 20 μm being frequently employed and with 10 μm being preferred. The distance between the bonding pads 13 can be set at about 10 μm. Even if the dummy interconnections 11 of such a size are formed, the parasitic capacitance of the interconnection 10 does not increase and therefore does not cause a problem of retarding a signal transferred to the interconnection 10. As a result, the performance of the logic integrated circuit device is not deteriorated.

[0104]The length (b) of each of the dummy interconnections 11 is set at not less than twice the minimum line width, and in the scribing area, it is set at not greater than the distance between the bonding pads, for example, not greater than

10 μm. When the width (b) and length (a) of each ~~of F~~ of the dummy interconnections 11 are each set at the minimum line width, there is a possibility that proper resolution of the dummy interconnections 11 will not be attained. By setting the length (b) at least twice the minimum line width, the resolution of the dummy interconnections 11 can be carried out with certainty even if the width (a) is the minimum line width, which makes it possible to process it with certainty. For the same reason in the width (a), the length (b) is set at, for example, not greater than the distance between bonding pads, for example, not greater than 10 *μm*. Similar to the width (a), the length (b) of each of the dummy interconnections 11 is constituted at not greater than 30 *μm*, with 20 μm or less being frequently employed and with 10 μm or less being preferred.

[0115]As illustrated in Fig. 5, on a semiconductor substrate 1, a shallow trench 2 is formed using photolithography and etching techniques. On the principal surface of the [[-semiconductor]] semiconductor substrate 1 having the shallow trench 2 formed therein, a silicon oxide film is deposited, and then, it is polished by the CMP method or the like to form an element isolation region 3. Then, N-type and P-type well regions may be formed.

[0118]As illustrated in Fig. 8, an insulating film ~~l2a~~ 12a is formed by the CVD method using TEOS. As the CVD method, a plasma CVD method can be employed, but a thermal CVD method using ozone in combination can be employed alternatively. The film thickness of the insulating film ~~l2a~~ 12a is set at 300 nm. Incidentally, Figs. 8 to 11 are cross-sectional views each illustrating only an interconnection layer and the layers therebelow are omitted.

[0121]As illustrated in Fig. 9, an insulating film ~~12c~~ 12c is then formed by the CVD method using TEOS. The insulating film 12 can be formed to have a film thickness of 700 nm. In the case where no dummy interconnection is disposed as is illustrated in Fig. 29, the thickness of the insulating film 12c is required to be about 1700 nm, but in Embodiment 1, the thickness can be decreased to 700 nm because of the presence of the dummy interconnections 11. As a result, the step for deposition the insulating film 12 can be shortened, whereby the step load can be reduced.

[0122]As illustrated in Fig. 10, the surface of the insulating film 12c is then polished by the CMP method and planarized. In Embodiment 1, the surface shape of the insulating film 12c reflects the shapes of the interconnections 10 and dummy interconnections 11, as well as that of the insulating film 12b, so that the insulating film 12c has substantially an even height at any place. As a result, the polishing rate becomes substantially uniform irrespective of the locations, whereby the surface of the insulating film 12c can be substantially planarized. In addition, the insulating film ~~12c~~ 12c has a film thickness as little as 700 nm, which makes it possible to reduce the CMP polishing amount and to reduce the load of the CMP polishing step. Incidentally, the polishing amount can be decreased to 200 nm.

[0123]Then, a surface washing after CMP polishing is effected, followed by the formation of an insulating film ~~12d~~ 12d by the CVD method-using TEOS; as is illustrated in Fig. 11. The insulating film ~~12d~~ 12d can be formed to have a thickness of 200 nm. Incidentally, it is possible to omit the insulating film 12d and to form the

insulating film 12c to have a thickness of 900 nm.

[0124] In this manner, the first interconnection layer is completed. Similar to the first interconnection layer, the second to fourth interconnection layers are then formed, followed by the formation of the fifth interconnection layer similarly. Over the fifth interconnection layer, a [[-passivation]] passivation film 25 is formed, whereby the logic integrated circuit device as illustrated in Fig. 1 is almost completed.

[0128]The logic integrated circuit device according to Embodiment 2 is substantially similar to that of Embodiment 1 except for the fifth interconnection layer. Accordingly, ~~dscription~~ description of the common features is omitted herein and only the differences will be described below.

[0144]Incidentally, the process for the fabrication of the DRAM of Embodiment 3 will next be described with reference to Figs. 18 to 21. Figs. 18 to 21 are [[cross—sectional]] cross-sectional views each illustrating one example of the fabrication process of the DRAM of Embodiment 3 in the order of the steps thereof.

[0155]As illustrated in Fig. 25, a silicon nitride film 61 is deposited on the principal surface of the semiconductor substrate 1, followed by the patterning of the silicon nitride film 61 and the semiconductor substrate 1 to form shallow trenches 2. The shallow trenches 2 include ~~boththose~~ both those which will be element isolation regions D,3 and those which are dummy regions 60. In other words, the shallow trenches 2 are formed so that the dummy regions 60 are disposed in the element isolation region D,3 which defines the active region 4.

[0156]As illustrated in FIG. 26, a silicon oxide film is deposited, for example, by the CVD method. As a first polishing, the resulting film is polished by the CMP method and embedded in the shallow trench 2, whereby the element isolation region D,3 and dummy regions 60 are formed. For the first polishing, an alkaline slurry containing silicon oxide particles as an abrasive can be employed. In this case, it is necessary to form the silicon oxide film to a certain thickness because a ratio of the polishing rate of the [[-silicon]] silicon oxide film to that of the silicon nitride film becomes 3 to 4:1.

[0161] For example, in the above Embodiments 1 to 4, the ~~CMPstep~~ CMP step serves as a step for polishing an insulating film. The present invention makes it possible to secure flatness to some extent prior to the CMP polishing so that the CMP polishing can be employed as a finishing step. In this case, not only the CMP method, but also dry-belt polishing or lapping method, can be adopted as the finishing step.